CLAIMS

1. A device intended to deliver an alarm signal upon detection of a gravitational wave generated by a body falling into a swimming pool, which comprises a means (10) of sensing aquatic waves that is placed beneath the surface of the water of the swimming pool, a means (13) of converting the aquatic waves sensed by said sensing means into an analogue electrical signal (S1), and a differential detector (14) that includes comparison means (20) for comparing the sensitivity threshold value of said differential detector with the value of said analogue electrical signal and to deliver said alarm signal when said analogue electrical signal exceeds said sensitivity threshold value, said differential detector comprising autoregulation means consisting mainly of an analogue/digital converter (36) that receives said preamplified analogue electrical signal as input and delivers a digital signal (S2) as output when a disturbance in the water occurs, a comparator (44), the "+" input of which receives said preamplified analogue electrical signal, and a microprocessor (38) programmed to deliver, in response to the detection of said digital signal delivered by said converter, a digital signal (S3) to the "-" input of said comparator, the output pulses (S4) of which have a variable width, which increases with the duration and with the magnitude of said disturbance so as to automatically increase the threshold for tripping an alarm means (16) and therefore to reduce the sensitivity of the device when said sensing means detects an atmospheric disturbance, such as wind;

said device being characterized in that said microprocessor triggers said alarm means when the width (TS4) of the output pulses (S4) from said comparator is larger than a predetermined critical reference (REF) and in that the frequency F of said analogue

electrical signal lies between two predetermined values F1 and F2.

2. The device as claimed in Claim 1, in which said microprocessor (38) assigns a sensitivity level (NS) to the device, said sensitivity level being incremented by 2 when the frequency F of said analogue electrical signal does not lie between said predetermined values F1 and F2 when the width (TS4) of the output pulses (S4) from said comparator (44) is larger than said predetermined critical reference (REF).

3. The device as claimed in Claim 2, in which said sensitivity level is incremented by 2 by said microprocessor (38) when the width (TS4) of the output pulses (S4) from said comparator lies between a second predetermined minimum reference (REF2) and said predetermined critical reference (REF).

4. The device as claimed in Claim 2, in which said sensitivity level is incremented by 2 by said microprocessor (38) when the value of the output pulses (S4) from said comparator (44) is equal to 0, while the value of the digital signal (S2) output by said analogue/digital converter (36) is not equal to 0 and when the width (TS2) of said digital signal is smaller than a first predetermined minimum reference (REF1).

5. The device as claimed in Claim 4, in which said differential detector (14) furthermore includes an autoregulation counter (50) that is actuated in order to decrement from a predetermined capacitance down to 0 or to increment from 0 up to said predetermined capacitance when, with the value of the output pulses (S4) from said comparator (44) being equal to 0, the value of the digital signal (S2) output by said analogue/digital converter (36) is not equal to 0

and its width (TS2) is smaller than said first minimum reference (REF1).

6. The device as claimed in Claim 3, in which said differential detector (14) furthermore includes an autoregulation counter (50) that is actuated by said microprocessor (38) in order to decrement from a predetermined capacitance down to 0 or increment said predetermined capacitance from 0 (counter = 0) when, the value of the output pulses (S4) from said comparator (44) being different from 0, their width (TS4) is smaller than said second predetermined minimum reference (REF2).

7. The device as claimed in Claim 5 or 6, in which said counter (50) is not actuated for decrementing or incrementing (counter = 0) when the value of the output pulses (S4) from said comparator (44) is equal to 0 and the value of the digital signal (S2) output by said analogue/digital converter (36) is equal to 0.

8. The device as claimed in Claim 7, in which, when it turns out that said autoregulation counter (50) has finished decrementing or incrementing (counter = 1), said sensitivity level (NS) is decremented by 1 by said microprocessor (38) and said counter is again actuated for decrementing or incrementing (counter = 0).

9. The device as claimed in one of Claims 1 to 8, which furthermore includes an autocalibration counter (52) that is actuated by said microprocessor (38) in order to decrement from a specified capacitance down to 0 or to increment from 0 up to said capacitance (counter = 0), an autocalibration of the device being carried out when said counter has finished decrementing or incrementing (counter = 1).

10. The device as claimed in Claim 9, in which the value of said signal (S3) delivered to the "-" input of said comparator (44) results from the charging of a capacitor (46) by pulses delivered by said microprocessor (38) during a time interval N, the autocalibration consisting in incrementing the value of N by 1 over a specified period as long as the values of the digital signal (S2) output by said analogue/digital converter (36) and of the output pulses (S4) from said comparator (44) are equal to 0.

11. The device as claimed in Claim 10, in which the value of N is decremented by 5 when the value of the digital signal (S2) output by said analogue/digital converter (36) is equal to 0 while the value of the output pulses (S4) from said comparator (44) is different from 0.

12. The device as claimed in one of Claims 1 to 11, in which said predetermined frequencies F1 and F2 are equal to 0.8 Hz and 1.2 Hz respectively.